IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants: Chi-Ming Tsai et al.

Assignee: Synopsys, Inc.

Title: METHOD FOR PROVIDING FLEXIBLE AND DYNAMIC REPORTING CAPABILITY USING SIMULATION TOOLS

Serial No.: 10/025,414 File Date: December 18, 2001

Examiner: Jason S. Proctor Art Unit: 2123

Docket No.: NTI-025

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November 14, 2005

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**APPEAL BRIEF**

Sir:

This Appeal Brief, filed in triplicate, is in support of the Notice of Appeal dated October 5, 2005.

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**INDEX**

## I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Synopsys, Inc., pursuant to the Assignments recorded in the U.S. Patent and Trademark Office on December 18, 2001 on Reel 012406, Frame 0304 and on February 2, 2005 on Reel 015653, Frame 0738.

## II. RELATED APPEALS AND INTERFERENCES

Based on information and belief, there are no other appeals or interferences that could directly affect or be directly affected by or have a bearing on the decision by the Board of Patent Appeals in the pending appeal.

## III. STATUS OF CLAIMS

Claims 1-20 are pending. Claims 1-20 stand rejected.

In the present paper, rejected Claims 1-20 are appealed.

Pending Claims 1-20 are listed in Appendix A.

## IV. STATUS OF AMENDMENTS

All amendments to the claims requested by Appellants were entered and are reflected in Appendix A.

## V. SUMMARY OF CLAIMED SUBJECT MATTER

To understand the context of and the problem solved by the invention, Appellants have provided paragraphs [0002]-[0006] of the Specification below. Appellants have provided paragraphs [0007]-[0008] of the Specification to summarize the invention.

> [0002] In sub-wavelength designs, traditional design rule checking (DRC) tools cannot be relied upon as a final check for silicon manufacturability. Specifically, because features can be distorted during the sub-wavelength manufacturing process due to both local and global proximity effects, DRC tools cannot provide the coverage and assurance needed for silicon sign-off.
>
> [0003] To resolve this problem, certain simulation tools have been provided that can verify the layout of a sub-wavelength integrated circuit compared to the printed wafer. Numerical Technologies, Inc. licenses such a tool, the SiVL® software package. This simulation tool can read in a user's layout and then simulate lithographic processes and conditions. The resulting simulated wafer image can be compared to the user's layout.
>
> [0004] Prior to this comparison step, the user is generally prompted to designate a tolerance, i.e. a maximum acceptable deviation, from the user's original layout. In one embodiment, the simulation tool can generate a graphical output including the original layout with contours showing the simulated wafer image. An area of the layout exceeding the tolerance can be marked with a graphical symbol, such as a "+" or "■". See, for example, U.S. Patent Application Serial No. 09/960,669, filed on September 21, 2001 by Numerical Technologies, Inc. Understanding where tolerance violations occur can indicate problems with the design or perhaps errors in providing rule parameters. However, setting a zero-tolerance can result in a large number of tolerance violations throughout the layout. Thus, setting the tolerance too tight generates too much information for a useful user review. Moreover, the appropriate tolerance can vary significantly from one design to another design. Therefore, determining an appropriate tolerance that

can provide useful simulation results is frequently a trial and error process.

[0005] Unfortunately, a new tolerance cannot leverage the results of a previous simulation. Specifically, setting a new tolerance requires repeating the simulation, thereby wasting considerable resources. For example, a medium-sized integrated circuit layout may take between 12 and 24 hours to simulate. Thus, the simulation tool is inefficiently used to re-run simulations on the same design rather than running new designs. Moreover, after this long process time, the user analysis done for proposing that specific tolerance may not be retained, thereby requiring further analysis. Thus, user time is also wasted on one design.

[0007] In accordance with one feature of the invention, a user can extract information from a database, which is generated by a one-time simulation of the user's layout. Specifically, designated control point information (e.g. a type, a rule identification, a tolerance, and a target parameter) and detailed deviation information regarding control points on the layout can be stored in the database. The user can tailor various reporting formats to provide the information most pertinent to that user.

[0008] Advantageously, based on the database, a user can easily change information regarding the rule identification, tolerance, and target parameter and still generate valid reports. Because a simulation on a layout need only be done once and accessing a database is significantly faster than simulating a layout, these reports can be expeditiously generated. This flexible and dynamic reporting capability provides the user with a rich source of information regarding the layout, thereby allowing that user to make better-informed decisions on correcting the layout.

## VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following issues are presented to the Board of Appeals for decision:

(A) Whether Claims 1-20 are patentable under 35 U.S.C. 102(b) over Lavenir CAM Software User's Guide (Lavenir).

## VII. ARGUMENTS

A. Claims 1-20 are patentable under 35 U.S.C. 102(b) over Lavenir CAM Software User's Guide (Lavenir)

1. Lavenir Overview

Lavenir teaches high-speed CAM software for printed circuit board (PCB) data. Page 13. Lavenir provides chapters to describe various aspects of this software. Pages 1-10. For example, Chapter 4 describes how to insert new plot data for the PCB, edit selected plot data, select elements for editing, etc. Pages 3-4. Chapter 11 describes two type of design rule checking routines: raster and vector DRC techniques. Pages 8 and 9.

2. Appellants' limitations recited in Claims 1-20 are not taught by Lavenir.

Claim 1 recites:

> A method of generating reports regarding an integrated circuit layout, the method comprising:
> providing a plurality of control points associated with the integrated circuit layout;
> performing a single simulation of the plurality of control points;
> storing information from the single simulation in a database, wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and
> extracting a subset of information from the database to generate the reports using a first set of checking parameters, wherein extracting is repeatable with a second set of checking parameters without repeating the steps of providing, performing, and storing.

Appellants respectfully submit that Lavenir fails to disclose or suggest the recited method. In general, Lavenir teaches CAM software for printed circuit board (PCB) data (page 13), not for generating a report for an integrated circuit (IC) layout. This distinction becomes increasingly clear upon closer examination of the limitations of the recited method. For example, because Lavenir teaches manipulating PCB data, Lavenir fails to disclose or suggest providing a plurality of control points associated with an IC layout.

Moreover, as taught by Appellants in paragraphs [0002] and [0003]:

> In sub-wavelength designs, traditional design rule checking (DRC) tools cannot be relied upon as a final check for silicon manufacturability. Specifically, because features can be distorted during the sub-wavelength manufacturing process due to both local and global proximity effects, DRC tools cannot provide the coverage and assurance needed for silicon sign-off.
>
> To resolve this problem, certain simulation tools have been provided that can verify the layout of a sub-wavelength integrated circuit compared to the printed wafer. Numerical Technologies, Inc. licenses such a tool, the SiVL® software package. This simulation tool can read in a user's layout and then simulate lithographic processes and conditions. The resulting simulated wafer image can be compared to the user's layout.

Because Lavenir teaches manipulating data at the board level, not at a sub-wavelength level, simulation is not necessary. Indeed, Lavenir does not once mention the word "simulation" within 516 pages. Therefore, Lavenir also fails to disclose or suggest performing a single simulation of the plurality of control points.

The Examiner argues that Appellants' previous traversal of the 35 U.S.C. 112 rejection contradicts the traversal of the current 35 U.S.C. 102(b) rejection. Appellants disagree. The

First Office Action of March 1, 2005 rejected Claims 1-6 and 17-20 as not being enabling. Specifically, that Office Action stated, "The simulation that produces data for parameters that are unknown or unspecified at the time of simulation is not enabled by the disclosure. Particularly lacking are the process by which the **inventive** simulation operates, the form taken by the simulation results, and how the database interface relates specified simulation parameters of the simulation data." (emphasis added)

The Amendment In Response To The First Office Action dated April 25, 2005 explained that Appellants recited database captures certain information about a simulation, thereby allowing a new tolerance to leverage the results of that simulation (in contrast to the prior art, e.g. paragraph [0005]). Specifically, a prior art simulation would output a graphical output including the original layout with contours showing the simulated wafer image. Paragraph [0004]. Areas of the layout exceeding a user-defined tolerance (which is requested before the simulation) are typically marked by graphical symbols. Paragraph [0004]. Appellants have described the state of the art in the Specification, paragraphs [0002]-[0005].

In contrast, as taught by Appellants in the Specification (emphasis added) with respect to the recited database,

> [0029] If the deviation of a control point is greater than its tolerance (as determined by simulation module 102), then the deviation of this control point can be written to the database. Of importance, **the actual magnitude of the deviation as well its the direction** (wherein "+" indicates a deviation outside the feature as defined by the original layout and a "-" indicates a deviation inside the feature) **can be written to the database.** Note that **in current simulation tools the presence and location of the deviation can be accessed. However,**

**the user is unable to access more in-depth information to facilitate more useful simulation results.**

Therefore, the simulation itself is not the object of Appellants' invention. Rather, the invention relates to a novel database that can capture information regarding that simulation to minimize the need to repeat the simulation process. For example, assume a user has designated 10 nm as the tolerance. In this case, a prior art simulation output could graphically show each location where a deviation greater than the tolerance occurs. However, if the user changes the tolerance to 11 nm, then another simulation must be performed to provide the new data. In contrast, the actual deviation (e.g. +12 nm) of a control point can be captured in Appellants' recited database. In this case, if the user changes the tolerance from 10 nm, the database can easily be searched to find any deviations greater than 10 nm (e.g. 11 nm, 12 nm, 13 nm, etc.).

As noted by Appellants,

> [0030] Because users tend to set tight tolerances, the database would typically store information regarding a significant subset of the control points in the layout. In this the manner, the time-consuming step of simulation need only be performed once to provide the information needed to generate the multitude of reports that could later be requested by the user. In accordance with one feature of the invention, the detailed control point information stored in the database allows the simulation tool to generate flexible and dynamic reporting of the simulation results.

The information in the database can be organized into various tables to facilitate reporting. Specification, paragraph [0034]. Exemplary tables are described in reference to Figures 3, 4, and 5.

Thus, as stressed above, it is the **stored information from the single simulation** that provides the advantage of extracting

information from the database using various checking parameters without repeating the steps of providing a plurality of control points, performing a simulation, and storing information from that simulation.

The Examiner in the Advisory Action seeks, in effect, to eliminate the limitation of performing the single simulation in Claim 1. Appellants submit that such elimination is impermissible. The stored database information is generated from the single simulation. Moreover, generating reports regarding the IC layout includes extracting subsets of information from that database. Therefore, the limitation of performing a single simulation cannot be eliminated from Claim 1.

Appellants note that the Examiner characterizes a vector design rule check as a simulation. Final Office Action dated July 19, 2005. Appellants traverse this characterization. As taught by Appellants, in sub-wavelength designs, traditional design rule checking (DRC) tools cannot be relied upon as a final check for silicon manufacturability. Specification, paragraph [0002]. For this reason, simulation tools were developed. Specification, paragraph [0003]. Therefore, design rule checking (DRC) is not the same as simulation.

Because Lavenir does not teach anything about a simulation, Lavenir must also logically fail to teach storing information from that simulation in a database. Additionally, the simulation information includes deviation information that indicates a deviation of a simulated location from a corresponding location on the IC layout. Lavenir teaches neither the simulated location nor the location on an IC layout. Appellants note that determining a clearance and contact between elements (Lavenir, page 385) for a PCB does not require a simulation.

Because Lavenir fails to disclose or suggest multiple elements of the recited method, Appellants request reconsideration and withdrawal of the rejection of Claim 1.

Claims 2-6 depend from Claim 1 and therefore are patentable for at least the reasons presented for Claim 1. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claims 2-6.

Moreover, Claim 2 recites, "wherein providing the plurality of control points includes designating at least one of a type, a rule identification, a tolerance, and a target parameter for each control point". Lavenir fails to disclose or suggest a tolerance for each control point associated with an IC layout. The Final Office Action cites the air gap violations (i.e. the system of Lavenir flags elements that are closer together than the minimum acceptable air gap) as teaching the recited tolerance for each control point. Appellants traverse this characterization. An air gap on a PCB does not teach anything about a tolerance for a control point on an integrated circuit. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 2.

Moreover, Claim 6 recites, "storing new information in the database based on the at least one new rule and the single simulation". Lavenir fails to disclose or suggest storing the information based in part on a simulation. The Final Office Action cites "Violations D Code" as teaching this new information. Appellants traverse this characterization. As recited, the new information must be based on the new rule(s) and the single simulation. Violations D Code does not teach anything about a simulation. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 6.

Claim 7 recites:

A database for reporting results from simulating an integrated circuit layout, the database comprising:

a plurality of control points associated with the integrated circuit layout;

information regarding the plurality of control points; and

deviation information regarding the plurality of control points, wherein the deviation information indicates deviations of simulated locations from corresponding locations on the integrated circuit layout, the deviation information including a magnitude of each deviation.

Therefore, Claim 7 is patentable for substantially the same reasons presented for Claim 1. That is, Lavenir fails to disclose an integrated circuit layout, much less deviations of simulated locations from corresponding location on that IC layout. The Final Office Action cites the "gap settings" (i.e. the system of Lavenir flags elements that are closer together than the minimum acceptable air gap) as teaching the recited deviation information of the plurality of control points. Appellants traverse this characterization. An air gap on a PCB does not teach anything about a magnitude of each deviation for a control point on an integrated circuit. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claim 7.

Claims 8-10 depend from Claim 7 and therefore are patentable for at least the reasons presented for Claim 7. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claims 8-10.

Moreover, Claim 8 recites, "further including a spacing for each control point related to an edge of the integrated circuit layout". Because Lavenir fails to teach anything about an IC layout, Lavenir cannot disclose or suggest spacing for each control point related to an edge of that IC layout. The Final Office Action cites the "outline to copper area" (i.e. the

system of Lavenir flags any copper area elements that are closer than the minimum acceptable distance to the board outline) as teaching the recited spacing for each control point. Appellants traverse this characterization. Spacing from a copper element to an edge of board does not teach anything about spacing for each control point related to an edge of an integrated circuit layout. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 8.

Moreover, Claim 9 recites, "wherein the information includes at least one of a type, a rule identification, a tolerance, and a target parameter for each control point". Because Lavenir fails to teach anything about a control point associated with an IC layout, Lavenir cannot disclose or suggest information about that control point. The Final Office Action cites pads and types of traces/arcs on the PCB as teaching type information about a control point. Appellants traverse this characterization. A pad, trace, or arc on a PCB cannot teach a control point associated with an integrated circuit layout. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 9.

Claim 11 recites:

> A method of generating simulation reports regarding an integrated circuit layout, the method comprising:
>
> dissecting feature edges on the integrated circuit layout into segments, each segment including a control point;
>
> performing a single simulation of the integrated circuit layout using the control points;
>
> storing simulation information in a database, wherein the simulation information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and
>
> extracting user-identified information from the database to generate the simulation reports.

Therefore, Claim 11 is also patentable for substantially the same reasons presented for Claim 1. That is, Lavenir fails to disclose or suggest anything about simulation reports regarding an IC layout, much less the recited steps of dissecting, performing, storing, and extracting to generate such simulation reports. The Final Office Action characterizes the Vector Design Rule Check as teaching dissecting feature edges on an IC layout into segments, performing the single simulation, and storing information from the single simulation in a database. The Final Office Action further characterizes the gap settings as teaching deviation information for at least one control point. Appellants traverse these characterizations. The Vector Design Rule Check and gap settings for a PCB teach nothing about the recited steps involving an IC layout. Based on the above reasons, Appellants request reconsideration and withdrawal of the rejection of Claim 11.

Claims 12-16 depend from Claim 11 and therefore are patentable for at least the reasons presented for Claim 11. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claims 12-16.

Moreover, Claim 12 recites, "further includes designating at least one of a type, a rule identification, a tolerance, and a target parameter for each control point". Because Lavenir fails to teach anything about a control point on a segment of a feature edge of an IC layout, Lavenir cannot disclose or suggest information about that control point. The Final Office Action cites pads, traces, and arcs on the PCB as teaching the type designation for a control point. Appellants traverse this characterization. Pads, traces, and arcs on a PCB cannot teach anything regarding control points, much less the designation of

such control points. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 12.

Moreover, Claim 16 recites, "further including providing at least one new rule associated with the control points and storing new information in the database based on the at least one new rule and the single simulation". Lavenir fails to disclose or suggest storing the information based in part on a simulation. The Final Office Action cites the Violations D Code and the Vector Design Rule Check as teaching this limitation. Appellants traverse this characterization. Neither the Violations D Code nor the Vector Design Rule Check teach anything about control points or a simulation. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 16.

Claim 17 recites:

> An apparatus for generating reports regarding an integrated circuit layout, the apparatus comprising:
> means for providing a plurality of control points associated with the integrated circuit layout;
> means for performing a single simulation of the plurality of control points;
> means for storing information from the single simulation in a database, wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and
> means for extracting a subset of information from the database to generate the reports using a first set of checking parameters, wherein extracting is repeatable with a second set of checking parameters without repeating the steps of providing, performing, and storing.

Therefore, Claim 17 is patentable for substantially the same reasons presented for Claim 1. That is, Lavenir fails to disclose reports regarding an IC layout, much less the means for performing a single simulation of control points associated with

that IC layout. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claim 17.

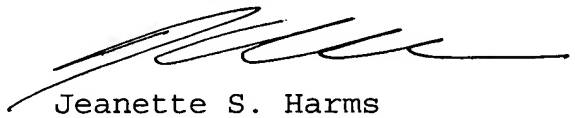
Claims 18-20 depend from Claim 17 and therefore are patentable for at least the reasons presented for Claim 17. Based on those reasons, Appellants request reconsideration and withdrawal of the rejection of Claims 18-20.

Moreover, Claim 18 recites, "means for designating at least one of a type, a rule identification, a tolerance, and a target parameter for each control point". Because Lavenir fails to teach anything about a control point on a segment of a feature edge of an IC layout, Lavenir cannot disclose or suggest information about that control point. Therefore, Appellants request further reconsideration and withdrawal of the rejection of Claim 18.

**B. CONCLUSION**

For the foregoing reasons, it is submitted that the Examiner's rejections of Claims 1-20 are erroneous, and reversal of these rejections is respectfully requested.

Respectfully submitted,



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## VIII. CLAIMS APPENDIX

1. (Previously Presented) A method of generating reports regarding an integrated circuit layout, the method comprising:

providing a plurality of control points associated with the integrated circuit layout;

performing a single simulation of the plurality of control points;

storing information from the single simulation in a database, wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and

extracting a subset of information from the database to generate the reports using a first set of checking parameters, wherein extracting is repeatable with a second set of checking parameters without repeating the steps of providing, performing, and storing.

2. (Original) The method of Claim 1, wherein providing the plurality of control points includes designating at least one of a type, a rule identification, a tolerance, and a target parameter for each control point.

3. (Original) The method of Claim 1, wherein storing information includes organizing the information in at least one of a main table, a statistics table, and a cell table.

4. (Previously Presented) The method of Claim 1, wherein extracting the subset of information includes creating a temporary table for the subset of information, wherein the temporary table is separate from the database.

5. (Previously Presented) The method of Claim 1, wherein extracting the subset of information includes viewing the subset of information in at least one of a sequential browse mode, a view by area mode, a histogram mode, an error count mode, and a Graphics Data Syntax (GDS mode).

6. (Original) The method of Claim 1, further including providing at least one new rule associated with the plurality of control points and storing new information in the database based on the at least one new rule and the single simulation.

7. (Previously Presented) A database for reporting results from simulating an integrated circuit layout, the database comprising:

a plurality of control points associated with the integrated circuit layout;

information regarding the plurality of control points; and

deviation information regarding the plurality of control points, wherein the deviation information indicates deviations of simulated locations from corresponding locations on the integrated circuit layout, the deviation information including a magnitude of each deviation.

8. (Previously Presented) The database of Claim 7, further including a spacing for each control point related to an edge of the integrated circuit layout.

9. (Previously Presented) The database of Claim 7, wherein the information includes at least one of a type, a rule identification, a tolerance, and a target parameter for each control point.

10. (Previously Presented) The database of Claim 7, wherein the information and the deviation information is organized in at least one of a main table, a statistics table, and a cell table.

11. (Previously Presented) A method of generating simulation reports regarding an integrated circuit layout, the method comprising:

dissecting feature edges on the integrated circuit layout into segments, each segment including a control point;

performing a single simulation of the integrated circuit layout using the control points;

storing simulation information in a database, wherein the simulation information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and

extracting user-identified information from the database to generate the simulation reports.

12. (Original) The method of Claim 11, further including designating at least one of a type, a rule identification, a tolerance, and a target parameter for each control point.

13. (Previously Presented) The method of Claim 11, wherein storing simulation information includes organizing information in at least one of a main table, a statistics table, and a cell table.

14. (Previously Presented) The method of Claim 11, wherein extracting user-identified information includes creating a

temporary table for user-identified information, wherein the temporary table is separate from the database.

15. (Previously Presented) The method of Claim 11, wherein extracting user-identified information includes viewing the user-identified information in at least one of a sequential browse mode, a view by area mode, a histogram mode, an error count mode, and a Graphics Data Syntax (GDS mode).

16. (Original) The method of Claim 11, further including providing at least one new rule associated with the control points and storing new information in the database based on the at least one new rule and the single simulation.

17. (Previously Presented) An apparatus for generating reports regarding an integrated circuit layout, the apparatus comprising:

means for providing a plurality of control points associated with the integrated circuit layout;

means for performing a single simulation of the plurality of control points;

means for storing information from the single simulation in a database, wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout; and

means for extracting a subset of information from the database to generate the reports using a first set of checking parameters, wherein extracting is repeatable with a second set of checking parameters without repeating the steps of providing, performing, and storing.

18. (Original) The apparatus of Claim 17, wherein the means for providing the plurality of control points includes means for designating at least one of a type, a rule identification, a tolerance, and a target parameter for each control point.

19. (Original) The apparatus of Claim 17, wherein the means for storing information includes means for organizing the information in at least one of a main table, a statistics table, and a cell table.

20. (Previously Presented) The apparatus of Claim 17, wherein the means for extracting the subset of information includes means for creating a temporary table for the subset of information, wherein the temporary table is separate from the database.

## IX. EVIDENCE APPENDIX

None.

## X. RELATED PROCEEDINGS APPENDIX

None.

PTO/SB/21 (09-04)
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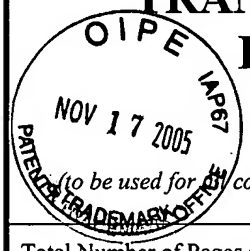


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| Total Number of Pages in This Submission | 25 |

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| **Application Number** | 10/025,414 |
| **Filing Date** | 12/18/2001 |
| **First Named Inventor** | Chi-Ming Tsai |
| **Art Unit** | 2123 |
| **Examiner Name** | Jason Scott Proctor |
| **Attorney Docket Number** | NTI-025 |

**ENCLOSURES** *(check all that apply)*

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# FEE TRANSMITTAL For FY 2005



☒ Applicant claims small entity status. See 37 C.F.R. § 1.27

**TOTAL AMOUNT OF PAYMENT** | **($) 500.00**

| *Complete if Known* | |
|---|---|
| Application Number | 10/025,414 |
| Filing Date | 12/18/2001 |
| First Named Inventor | Chi-Ming Tsai |
| Examiner Name | Jason Scott Proctor |
| Art Unit | 2123 |
| Attorney Docket No | NTI-025 |

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| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
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| | | Small Entity | | Small Entity | | Small Entity | |
| **Application Type** | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | **Fees Paid ($)** |
| **Utility** | 300 | 150 | 500 | 250 | 200 | 100 | $ |
| **Design** | 200 | 100 | 100 | 50 | 130 | 65 | $ |
| **Plant** | 200 | 100 | 300 | 150 | 160 | 80 | $ |
| **Reissue** | 300 | 150 | 500 | 250 | 600 | 300 | $ |
| **Provisional** | 200 | 100 | 0 | 0 | 0 | 100 | $ |

### 2. EXCESS CLAIM FEES

| **Fee Description** | Fee($) | Small Entity Fee($) |
|---|---|---|
| Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent | 50 | 25 |
| Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent | 200 | 100 |
| Multiple dependent claims | 360 | 180 |

| Total Claims | Extra Claims | Fee($) | **Fee Paid ($)** | Multiple Dependent Claims | |
|---|---|---|---|---|---|
| | - 20 or HP = | x | = | Fee($) | Fee($) |

HP = highest number of total claims paid for, if great than 20

| Indep. Claims | Extra Claims | Fee($) | **Fee Paid ($)** |
|---|---|---|---|
| | - 3 or HP = | x | = |

HP = highest number of total claims paid for, if great than 3

### 3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 USC 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | Extra Sheets | Number of each additional 50 or fraction thereof | Fee($) | Fee Paid ($) |
|---|---|---|---|---|
| - 100 = | 5- = (round up to a whole number) x | | = | |

### 4. OTHER FEE(S)

| | Fee Paid ($) |
|---|---|
| Non-English Specification - $130 fee (no small entity discount) | |
| Other: **APPEAL BRIEF** | **$500.00** |

**SUBMITTED BY**

| | | | |
|---|---|---|---|
| **Signature:** | Registration No. 35,537 | Telephone: | (408) 451-5907 |
| Name (Print/Type) Jeanette S. Harms | | Date: | November 14, 2005 |